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EXAMINER	
ELALLAM, AHMED	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,921	KOSONEN ET AL.	
	Examiner	Art Unit	
	AHMED ELALLAM	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is responsive to RCE filed on 05/252006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 26 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurihara, US (5,500,939).

Regarding claim 26, with reference to figure 1 and 3, Kurihara discloses an apparatus comprising:

Memory 2, (claimed means for receiving input data, means for storing said input data),

FIFO buffers 5, each connected to bus 3 and to the memory 2, (claimed means for receiving data from said means for storing said input data)

A controller 1, for setting a flag for indicating that all the FIFO memories became available to receive data from memory 2 (see figure 3, S8 and S9). (Claimed means for determining whether all of the means for receiving said data from said means for storing said input data have signalized their capability of receiving said data, and for repeating said determining until a corresponding indication of the capability of receiving

data has been received from all the means for receiving said data from said means for storing said input data), the controller further control the data from memory to be written to all the FIFO memories 5, see figure 3, step 9 (claimed means for releasing a transmission from said means for storing said input data to said means for receiving said data from said means for storing said input data, when all of said means for receiving data from said means for storing said input data have signalized their capability of receiving data).

Examiner interpreted the similarities of processors 6 connected to the FIFO(s) 5 to be the claimed means for storing said input data respectively connected to means for connecting to means for having the same interface address allocated.

Regarding claim 27, as indicated above, Kurihara discloses the controller for setting a flag for indicating that all the FIFO memories became available to receive data from memory 2 (see figure 3, S8 and S9). In addition Kurihara discloses if all buffers are ready, the controller 1 writes the attribute data into the FIFO memories 5 and if any one of the FIFO memories 5 has insufficient space to receive the attribute data, the controller suspends the write operation until every one of the FIFO memories 5 has sufficient free space to receive the attribute data. (means for receiving a control signal indicating the receiving capability from anyone of said means for receiving data from said means for storing said input data, and means for supplying a release signal to said means for storing said input data, when said control signal has been received from all of said means for receiving data from said means for storing said input data).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park US (6,430,197) in view of Ogimoto et al, US (6,032,205). Hereinafter referred to as Park and Ogimoto respectively.

Regarding claim 1, with reference to figure 2, Park discloses a method for supplying input data received from the ATM device 100 to the plurality of physical devices 610-640, wherein ATM cells transmission between the ATM layer device and the physical devices is carried out using UTOPIA level 1 interface, see column 10, lines 23-28, (the use of the UTOPIA level 1 interface reads on the protocol layer devices having the same interface address allocated), Park also discloses a prior art method (figure 1) in which an input buffer 20 is provided for connecting to an input channel and a plurality of output buffers (1-N) that are connected to a plurality of output channel (in accordance with UTOPIA level 2). See column 1, lines 2-43. (Claimed providing an input buffer connected to an input channel and a plurality of output buffers respectively connected to plurality of output channels connected to a plurality of physical protocol layers having the same interface address allocated). In addition Park discloses generating a signal for physical devices 610-640 can receive cells, see column 4, lines

54-60, (it is inherent that each physical device has an input buffer (claimed output buffer) because it needed for indicating the capability of the physical device to receive the data and/or to temporarily store data for further processing).

While Park teaches the indication from all the physical devices 610-640 to receive data (inherently based on the capacity of each physical device's buffer to receive data), it does not teach determining whether all of the output buffers have signalized their capability of receiving data, and if not repeating determining step until a corresponding indication of capability of receiving data has been received from all output buffers, and releasing transmission of input data from input buffer to the plurality of output buffers, when all the plurality of output buffers have signaled their capability of receiving data.

However, Ogimoto teaches determining whether all of the output buffers have signalized their capability of receiving data (using control means 122-125 as in claim 8), and if not repeating determining step until a corresponding indication of capability of receiving data has been received from all output buffers, and releasing transmission of input data from input buffer to the plurality of output buffers, when all the plurality of output buffers have signaled their capability of receiving data. See abstract, figure 1, 2.

It would have been obvious to a person of ordinary skill in the art, at the time the invention was made to combine the teaching of Park's method with the releasing of input buffer transmission to output buffers taught by Ogimoto so that UTOPIA 1 level interface demultiplexing between the ATM device and physical devices of Park can be implemented on the physical devices and ATM layer devices of prior art system (Park,

figure 1). The advantage would be the ability to have faster data transfer between the ATM and physical devices. It would be also advantageous to reduce cost by using the UTOPIA level 1 standard for already installed UTOPIA level 2 standard devices of prior art. (Park, column 10, lines 23-28).

Regarding claim 8 and 28, with reference to figure 2, Park discloses an apparatus for supplying input data received from the ATM device 100 to the plurality of physical devices 610-640, wherein the transmission of ATM cells between the ATM layer device and the physical devices is carried out using UTOPIA level 1 interface, see column 10, lines 23-28, (the use of the UTOPIA level 1 interface reads on the protocol layer devices having the same interface address allocated), Park also discloses a prior art apparatus (figure 1) in which an input buffer 20 is provided for connecting to an input channel (claimed input buffer configured to receive data) and a plurality of output buffers 1-N are connected to a plurality of output channel (in accordance with UTOPIA level 2). See column 1, lines 2-43. (Claimed an input buffer configured to store input data, a plurality of output buffers configured to receive data from the input buffer respectively connected to plurality of output channels, wherein the plurality of output channels are connected to a plurality of physical protocol layer devices having the same interface address allocated). In addition Park discloses generating a signal for physical devices 610-640 can receive cells, see column 4, lines 54-60, (it is inherent that each physical device has an input buffer (claimed output buffer) because it needed for indicating the capability of the physical device to receive the data and/or to temporarily store data for further processing).

While Park shows decoding/demultiplexing unit 400 (figure 2) (claimed controller) and teaches that the indication from all the physical devices 610-640 to receive data (inherently based on the capacity of each physical device's buffer to receive data), but does not teach a controller for determining whether all of the output buffers have signalized their capability of receiving data, and if not repeating determining step until a corresponding indication of capability of receiving data has been received from all output buffers, and releasing transmission of input data from input buffer to the plurality of output buffers, when all the plurality of output buffers have signaled their capability of receiving data.

However, Ogimoto teaches determining whether all of the output buffers have signalized their capability of receiving data and if not repeating determining step until a corresponding indication of capability of receiving data has been received from all output buffers, and releasing transmission of input data from input buffer to the plurality of output buffers, when all the plurality of output buffers have signaled their capability of receiving data. See abstract, figure 1, 2 and column 13, lines 33-49.

It would have been obvious to a person of ordinary skill in the art, at the time the invention was made to configure the controller of Park to implement the releasing of input buffer transmission to output buffers taught by Ogimoto so that UTOPIA 1 level interface demultiplexing between the ATM device and physical devices of Park can be implemented on the physical devices and ATM layer devices of prior art system (Park, figure 1). The advantage would be the ability to have faster data transfer between the ATM and physical devices. It would be also advantageous to reduce cost by using the

UTOPIA level 1 standard for already installed UTOPIA level 2 standard devices of prior art. (Park, column 10, lines 23-28).

Regarding claims 2 and 9, Park discloses that the buffers of multiplexing demultiplexing units are FIFO buffers, see figure2, 3,column 5, lines 37-53.

Regarding claims 3, 5, 6, 16 18,19, Park discloses the plurality of the physical protocol layer devices are UTOPIA level 1 compliant (as in claims 3 and 16), and the input channel is connected to the ATM device (as in claim 5 and 18), and the ATM device is UTOPIA level 1 device (as in claims 6,19). See column 10, lines 23-28.

Regarding claims 4 and 17, Park discloses the physical devices for receiving ATM cells, and all the devices are UTOPIA level 1, see column 10, lines 23-28.

Regarding claims 10 and 21, as discussed above, Park discloses the decoding/demultiplexing unit 400 (figure 2) (controller) for generating a signal indicating that first to fourth physical layer devices 610 to 640 can receive cells, see column 4, lines 54-60. Park does not specify the unit 400 supply a release signal to input buffer when the control signal has been received from all the plurality of output buffer means.

Ogimoto as discussed above, teaches releasing transmission of input data from input buffer to plurality of output buffers, when all of the plurality of output buffers are capable of receiving data. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made to enable the unit 400 to supply a release signal to input buffer when the control signal has been received from all the plurality of output buffers. A person of skill in the art would do so for implementing the respective method of Park in view Ogimoto as indicated in claim 1.

Regarding claim 11-14, 22-24, Park discloses the input channel is connected to the ATM device (as in claims 11 and 22), the ATM device is UTOPIA level 1 device (as in claim12), the plurality of the physical protocol layer devices are UTOPIA level 1 compliant (as in claims 13 and 23), and the output channel are connected to a plurality of ATM devices having the same interface address allocated (as in claims 14 and 24), (the physical devices are ATM devices). See column 10, lines 23-28.

Regarding claims 7, 15, 20 and 25, claims 7 and 20 are a multiplexing method having steps of providing communication from the physical devices to the ATM device, claims 15 and 25 are a multiplexing apparatus having elements for providing communication from the physical devices to the ATM device. In addition:

As to claims 7 and 20 Park discloses a prior art system (figure1) in which a multiplexing take place in which the plurality of output buffers (in case of demultiplexing) connected to the physical layer devices becomes input buffers (in case of multiplexing) and the input buffer connected to the ATM device (in case of demultiplexing) becomes output buffer (in case of multiplexing), see column 1, lines 66-67 and column 2, lines 1-43. (Claimed using output buffers as a plurality of input buffers respectively connected to the plurality of input channels, and using the input buffer (301) as an output buffer connected to output channel, storing received input data in a respective one of the plurality of input buffers and releasing transmission of the input data from the respective one of the plurality of input buffers to the output buffer, when the output buffer is capable of receiving data).

As to claim 15 and 25, claims 15 and 25 are apparatus claims having substantially the same scope of claims 7 and 20, thus they are subject to the same rejections.

Response to Arguments

3. Applicant's arguments filed 5/25/2006 have been fully considered but they are not persuasive:

Applicants argue that there is no mention or suggestion in Ogimoto of requiring all output buffers to have signalized the capacity of receiving data, and only if this condition occurs for all the output buffers is there a release of transmission of input data from an input buffer to a plurality of output buffers, as recited in claim 1.Examiner respectfully disagrees, Ogimoto discloses in the abstract:

"The vacant capacity of each output buffer is monitored to ensure that it is sufficiently high to store the broadcast message... The message transmission-permit signal is issued to the packet selector circuits only when the broadcast transmission-permit signals for all the output ports for transmitting the message are issued. The broadcast transmission-permit signals are issued only when the vacant capacity of each output buffer is sufficiently high to store a broadcast message".

From the above it is clear that the teaching of Ogimoto in which "the broadcast transmission-permit signals are issued only when **the vacant capacity of each output buffer is sufficiently high to store a broadcast message"** can be interpreted to mean "all output buffers to have signalized the capacity of receiving data".

Applicant further argued, *"Ogimoto is not analogous art, and therefore can not be relied upon in the rejection of claim 1. In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem*

with which the inventor was concerned. MPEP § 2141 .01(a); In re Oetiker, 24 USPQZd 1443, 1445 (Fed. Cir. 1992). Ogimoto is not in the field of the applicant's endeavor, but instead is in the field of a crossbar switch for a parallel computer. Ogimoto is therefore not reasonably pertinent to the particular problem with which the applicant of the current application is concerned. A reference is considered reasonably pertinent if it is one that would have logically commended itself to an inventor's attention in considering his problem. In re Clay, 23 USPQZd 1058, 1061 (Fed. Cir. 1992). Ogimoto is not analogous art, and thus cannot be used as a reference, and since the Office action admits that Park fails to disclose or suggest all the limitations of claim 1, claim 1 is further patentable over the cited references. Therefore, applicant respectfully requests that the rejection of claim 1 be withdrawn". Emphasis added.

In response to applicant's argument that *Ogimoto* is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, claim 1 as amended is in the same field of endeavor as far as buffer management is concerned, and since *Ogimoto* solve the same problem of buffering data between input and output buffers it is considered pertinent.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AHMED ELALLAM whose telephone number is (571) 272-3097. The examiner can normally be reached on 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, To Doris can be reached on (571) 272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A. E
Examiner
Art Unit 2616
6/24/06

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER